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| 10/763,903 | 01/23/2004 | Werner Harter | 10191/3523 | 7765 |

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| EXAMINER | |
|---|---|
| PUENTE, EMERSON C | |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/763,903 | HARTER, WERNER | |
| | Examiner | Art Unit | |
| | Emerson C. Puente | 2113 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *01 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-14 and 16-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18* is/are allowed.

6)☒ Claim(s) *1-14,16 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This action is made **Final.**

Claims 1-14 and 16-18 have been examined. Claim 15 has been canceled. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.

### *Claim Objections*

Claim 13 are objected to because of the following informalities:

In regards to claim 13, please change "the at least two processor unit" to "the at least two processor units".

Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-5,7,8,10,11, 13,14,16, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Douskey et al. referred hereinafter "Douskey" in view of US Patent No. 7,111,213 of Dastidar et al. referred hereinafter "Dastidar" and US Patent No. 6,868,309 of Begelman et al. referred hereinafter "Begelman".

In regards to claim 1, Douskey discloses a system having at least one computer device for applications critical with regard to safety, comprising:

at least two processor units. Douskey discloses an integrated circuit comprising a plurality of cores, wherein each core may include a predefined circuit arrange for performing one or more task, such as a processor core (see figure 2 and column 6 lines 24-35);

a memory unit for storing process data. Douskey discloses an integrated circuit comprising a plurality of cores, wherein each core may include a predefined circuit arrange for performing one or more task, such as a embedded memory (see figure 2 and column 6 lines 24-35);

a memory management unit for controlling memory accesses in the at least one computer device. Douskey discloses a system interface unit (SIU) having an external function access port (see column 6 lines 25-31). In the instance that one of the core is an embedded memory, the SIU constitute a memory management unit for controlling memory accesses to that core.

an error detection unit for detecting errors in the memory unit. Douskey further discloses a core interface unit (CIU) can be configured as an array built in self test (ABIST) controller that is used to perform testing of array elements such as embedded memories (see column 7 lines 48-52).

at least one self-test unit assigned to each of the at least two processor units. Douskey further discloses a core interface unit (CIU) can be configured as an logic built in self test (LBIST) controller that is used to perform testing of logic circuitry, such as processors, within a core (see column 2 lines 25-30 and column 7 lines 48-52).

a first connection means for connecting the at least two processor units to each other and a second connection means for connecting the at least two processor units to the memory management unit, the at least two processor units being positioned together with the memory unit on a shared chip surface area. Douskey discloses buses connecting the system interface unit with each of the cores, wherein some of the core may be processor cores (column 6 lines 28-35 and column 7 lines 17-20). Douskey also discloses wherein the cores, which may include processor cores and embedded memory are incorporated within an integrated circuit device or chip (see column 6 lines 24-26 and 32-35).

However, Douskey fails to explicitly disclose:

wherein at least one self test unit is configured to cyclically test the at least two processor units.

wherein at least two processor units exchange at least one of starting values, intermediate results, intermediate values, and final results via the connection means, and wherein the at least two processor units continuously check the at least one of starting values, intermediate results, intermediate values, and final results for uniformity.

Dastidar discloses performing built in self-test on a PLD or integrated circuit (see column 2 lines 30-32, column 3 lines 27-31). Datidar further discloses performing the test periodically or cyclically to ensure all logical elements are operable (see column 4 lines 13-15).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Douskey and Dastidar wherein the at least one self test unit is configured to cyclically test the at least two processor units. A person of ordinary skill in the art would have been motivated to combine the teachings because Douskey is concerned with

a built in self test unit testing an integrated circuit (see column 6 lines 1-3 and column 7 lines 46-48) and periodically or cyclically testing, as per teachings of Dastidar, constitutes a suitable known means of testing that ensures the logic elements or processor units remain operable (see column 4 lines 13-15).

Begelman further discloses redundant processors, wherein the redundant processors may compare each other's computational results during normal operations when executing command instructions and if the results between the processors differ, then the processors may perform self test to determine the faulty processor (see column 9 lines 25-30).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Douskey, Dastidar, and Begelman to include redundant processors, wherein the redundant processors may compare each other's computational results during executing command instructions and if the results between the processors differ, then the processors may perform self test to determine the faulty processor, indicating wherein at least two processor units exchange at least one of starting values, intermediate results, intermediate values, and final results via the connection means, and wherein the at least two processor units continuously check the at least one of starting values, intermediate results, intermediate values, and final results for uniformity. A person of ordinary skill in the art would have been motivated to combine the teachings because Douskey discloses a data processing system comprising processor cores (see column 6 lines 32-35), and as such, is concerned being able to process data, and having the processors redundant, as per teachings of Begelman, ensures no single point of failure, thus permitting continued operations or data processing upon failure to one processor (see column 1 lines 34-35 and 46-48).

In regards to claim 3, Douskey in view of Dastidar and Begelman discloses the claim limitation as discussed above. Douskey further discloses wherein each processor unit is assigned a self-test unit for performing a self-test. Douskey discloses a CIU, or self test unit, disposed in each of the cores (see column 7 lines 18-20) and further discloses the cores may be processor cores (see column 6 lines 32-35).

In regards to claim 4, Douskey in view of Dastidar and Begelman discloses the claim limitation as discussed above. Douskey further discloses two processor units are coupled by the connection means, each processor unit being assigned a self-test unit. Douskey discloses a bus connecting each of the cores, wherein some of the core may be processor cores (column 6 lines 24-35) and a CIU, or self test unit, disposed in each of the cores (see column 7 lines 18-20).

In regards to claim 5, Douskey in view of Dastidar and Begelman discloses the claim limitation as discussed above. Douskey further discloses wherein a plurality of computer devices are connected to one another with the aid of at least one connection unit, the plurality of the computer devices having one of an equal and different number of processor units. Douskey discloses the system may be implemented as more than one integrated circuit device, wherein each integrated circuit device may implement a multicore design (see column 5 lines 60-65).

In regards to claim 7, Douskey in view of Dastidar and Begelman discloses the claim limitation as discussed above. Douskey further discloses wherein the memory management unit for controlling the memory access in the at least one computer device and the at least one processor unit are implemented integrally as a single unit. Douskey discloses an integrated circuit connecting the system interface unit with each of the cores, wherein some of the core may be processor cores (column 6 lines 24-35).

In regards to claim 8, Douskey discloses a method for process-data processing in at least one computer device having at least two processor unit for applications critical with regard to safety, comprising:

testing the at least two processor units using at least one self-test unit assigned to each of the at least two processor units. Douskey further discloses a core interface unit (CIU) can be configured as an logic built in self test (LBIST) controller that is used to perform testing of logic circuitry, such as processors, within a core (see column 2 lines 25-30 and column 7 lines 48-52).

positioning the at least two processor units together with a memory unit on a shared chip surface area. Douskey also discloses wherein the cores, which may include processor cores and embedded memory are incorporated within an integrated circuit device or chip (see column 6 lines 24-26 and 32-35)

connecting the at least two processor units to each other using a first connection means and to a memory management unit using a second connection means in the at least one computer device. Douskey discloses a bus connecting the system interface unit with each of the cores, wherein some of the core may be processor cores (column 6 lines 28-35).

controlling memory accesses in the at least one computer device using the memory management unit. Douskey discloses a system interface unit (SIU) having an external function access port (see column 6 lines 25-31). In the instance that one of the core is an embedded memory, the SIU constitute a memory management unit for controlling memory accesses to that core.

storing process data in the memory unit. Douskey discloses an integrated circuit comprising a plurality of cores, wherein each core may include a predefined circuit arrange for

performing one or more task, such as a embedded memory (see figure 2 and column 6 lines 24-35);

detecting errors in the memory unit using an error detection unit. Douskey further discloses a core interface unit (CIU) can be configured as an array built in self test (ABIST) controller that is used to perform testing of array elements such as embedded memories (see column 7 lines 48-52).

However, Douskey fails to explicitly disclose:

testing cyclically;

the at least two processor units exchanging at least one of starting values, intermediate results, intermediate values, and final results via the connection means, and the at least two processor units continuously checking the at least one of starting values, intermediate results, intermediate values, and final results for uniformity.

Dastidar discloses performing built in self-test on a PLD or integrated circuit (see column 2 lines 30-32, column 3 lines 27-31). Datidar further discloses performing the test periodically or cyclically to ensure all logical elements are operable (see column 4 lines 13-15).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Douskey and Dastidar wherein the at least one self test unit is configured to cyclically test the at least two processor units. A person of ordinary skill in the art would have been motivated to combine the teachings because Douskey is concerned with a built in self test unit testing an integrated circuit (see column 6 lines 1-3 and column 7 lines 46-48) and periodically or cyclically testing, as per teachings of Dastidar, constitutes a suitable

known means of testing that ensures the logic elements or processor units remain operable (see column 4 lines 13-15).

Begelman further discloses redundant processors, wherein the redundant processors may compare each other's computational results during normal operations when executing command instructions and if the results between the processors differ, then the processors may perform self test to determine the faulty processor (see column 9 lines 25-30).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Douskey, Dastidar, and Begelman to include redundant processors, wherein the redundant processors may compare each other's computational results during executing command instructions and if the results between the processors differ, then the processors may perform self test to determine the faulty processor, indicating the at least two processor units exchanging at least one of starting values, intermediate results, intermediate values, and final results via the connection means, and the at least two processor units continuously checking the at least one of starting values, intermediate results, intermediate values, and final results for uniformity. A person of ordinary skill in the art would have been motivated to combine the teachings because Douskey discloses a data processing system comprising processor cores (see column 6 lines 32-35), and as such, is concerned being able to process data, and having the processors redundant, as per teachings of Begelman, ensures no single point of failure, thus permitting continued operations or data processing upon failure to one processor (see column 1 lines 34-35 and 46-48).

In regards to claim 10, Douskey in view of Dastidar and Begelman discloses the claim limitation as discussed above. Douskey further discloses wherein two processor units, coupled by

the first connection means, are each tested by assigned self-test units in the at least one computer device. Douskey discloses a bus connecting the system interface unit with each of the cores, wherein some of the core may be processor cores (column 6 lines 24-35) and a CIU, or self test unit, disposed in each of the cores (see column 7 lines 18-20).

In regards to claim 11, Douskey in view of Dastidar and Begelman discloses the claim limitation as discussed above. Douskey further discloses wherein at least two computer devices having one of an equal and different number of processor units are combined using at least one connection unit. Douskey discloses the system may be implemented as more than one integrated circuit device, wherein each integrated circuit device may implement a multicore design (see column 5 lines 60-65).

In regards to claim 13, Douskey in view of Dastidar and Begelman discloses the claim limitation as discussed above. Douskey further discloses wherein the at least two processor units is tested using an assigned self-test unit. Douskey discloses a CIU, or self test unit, disposed in each of the cores (see column 7 lines 18-20) and further discloses the cores may be processor cores (see column 6 lines 32-35).

In regards to claim 14, Douskey in view of Dastidar and Begelman discloses the claim limitation as discussed above. Douskey further discloses wherein the self-test unit outputs an error message via self-test unit output means to at least one of an external display unit and an error processing unit if a fault is recognized in the at least one processor unit by the assigned self-test unit. Douskey discloses outputting an ATTN signal, indicating an error message, from the CIUs, or self test units, to flag errors, wherein the ATTN signal is outputted to the master

interface unit connected to the service processor, indicating an error processing unit (see column 8 lines 29-34).

In regards to claim 16, Douskey in view of Dastidar and Begelman discloses the claim limitation as discussed above. Begelman further discloses wherein one of the at least two processor units outputs an error message via processor unit output means to at least one of an external display unit and an error processing unit if the one of the at least two processor units detects a deviation between the final results and one of the intermediate results and intermediate values. Begelman discloses when the results differ, performing a self test of the processors, wherein the proper functioning processor takes control and resets the failed processor (see column 9 lines 28-30).

In regards to claim 17, Douskey in view of Dastidar and Begelman discloses the claim limitation as discussed above. Douskey further discloses wherein, if errors occur in the memory unit, an error message is output via error detection unit output means to at least one of an external display unit and an error processing unit. Douskey discloses outputting an ATTN signal, indicating an error message, from the CIUs, or error detection unit in the case where the core is memory, to flag errors, wherein the ATTN signal is outputted to the master interface unit connected to the service processor, indicating an error processing unit (see column 8 lines 29-34).

Claims 2,6,9, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Douskey in view of Dastidar and Begelman and in further view of US Patent No. 5,313,424 of Adams et al. referred hereinafter "Adams".

In regards to claim 2, Douskey in view of Dastidar and Begelman discloses the claim limitation as discussed above.

However, Douskey in view of Dastidar and Begelman fails to explicitly disclose wherein the error detection unit is implemented as an error correction unit for correcting errors in the memory unit.

Adams discloses ABIST systems are known to use ECC techniques for correcting error founds in memory (see column 1 lines 34-38).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Douskey, Dastidar, Begelman, and Adams wherein the ABIST, as disclosed in Douskey, further include ECC techniques, indicating wherein the error detection unit is implemented as an error correction unit for correcting errors in the memory unit. A person of ordinary skill in the art would have been motivated to combine the teachings because Douskey is concerned with testing memory devices via an ABIST (see column 7 lines 49-52), and ECC techniques, as per teachings of Adams, are known to be used in ABIST systems for correcting error founds in memory (see column 1 lines 34-38). Adams further discloses using a self testing and self repairing system lower the cost of making memories by reducing testing expenses and improving memory yields (see column 1 lines 30-34).

In regards to claim 6, Douskey in view of Dastidar and Begelman discloses the claim limitation as discussed above. However, Douskey in view of Dastidar and Begelman fails to explicitly disclose wherein each memory unit is assigned one error correction unit in the at least one computer device.

Adams discloses ABIST systems are known to use ECC techniques for correcting error founds in memory (see column 1 lines 34-38).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Douskey, Dastidar, Begelman, and Adams wherein the ABIST, as disclosed in Douskey, further include ECC techniques, indicating wherein each memory unit is assigned one error correction unit in the at least one computer device. A person of ordinary skill in the art would have been motivated to combine the teachings because Douskey is concerned with testing memory devices via an ABIST (see column 7 lines 49-52), and ECC techniques, as per teachings of Adams, are known to be used in ABIST systems for correcting error founds in memory (see column 1 lines 34-38). Adams further discloses using a self testing and self repairing system lower the cost of making memories by reducing testing expenses and improving memory yields (see column 1 lines 30-34).

In regards to claim 9, Douskey in view of Dastidar and Begelman discloses the claim limitation as discussed above. However, Douskey in view of Dastidar and Begelman fails to explicitly disclose wherein errors in the memory unit are corrected using an error correction unit.

Adams discloses ABIST systems are known to use ECC techniques for correcting error founds in memory (see column 1 lines 34-38).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Douskey, Dastidar, Begelman, and Adams wherein the ABIST, as disclosed in Douskey, further include ECC techniques, indicating wherein errors in the memory unit are corrected using an error correction unit. A person of ordinary skill in the art would have been motivated to combine the teachings because Douskey is concerned with testing

memory devices via an ABIST (see column 7 lines 49-52), and ECC techniques, as per teachings of Adams, are known to be used in ABIST systems for correcting error founds in memory (see column 1 lines 34-38). Adams further discloses using a self testing and self repairing system lower the cost of making memories by reducing testing expenses and improving memory yields (see column 1 lines 30-34).

In regards to claim 12, Douskey in view of Dastidar and Begelman discloses the claim limitation as discussed above. However, Douskey in view of Dastidar and Begelman fails to explicitly disclose wherein the memory unit in the at least one computer device is checked for errors and corrected using an assigned error correction unit.

Adams discloses ABIST systems are known to use ECC techniques for correcting error founds in memory (see column 1 lines 34-38).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Douskey, Dastidar, Begelman, and Adams wherein the ABIST, as disclosed in Douskey, further include ECC techniques, indicating wherein the memory unit in the at least one computer device is checked for errors and corrected using an assigned error correction unit. A person of ordinary skill in the art would have been motivated to combine the teachings because Douskey is concerned with testing memory devices via an ABIST (see column 7 lines 49-52), and ECC techniques, as per teachings of Adams, are known to be used in ABIST systems for correcting error founds in memory (see column 1 lines 34-38). Adams further discloses using a self testing and self repairing system lower the cost of making memories by reducing testing expenses and improving memory yields (see column 1 lines 30-34).

### *Allowable Subject Matter*

Claim 18 is allowed for reasons stated in the previous office action.

### *Response to Arguments*

Applicant's arguments filed June 1, 2007 are moot in view of new ground(s) of rejection presented in this Office action.

### *Conclusion*

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emerson C. Puente whose telephone number is (571) 272-3652. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emerson Puente
Examiner
AU 2113